

## ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit and method for compressing test stimuli to one test output signal during a test mode. The test output signal is driven from one input/output node of the semiconductor integrated circuit to a test station through a load board interface. Buffer circuitry on the semiconductor integrated circuit drive a high impedance to the input/output nodes of the integrated circuit during the test mode. The load board interface allows a single test station to receive test output signals from a plurality of semiconductor integrated circuits of the invention during the test mode, thereby allowing one test station to simultaneously test a plurality of circuits.

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